भारतीय प्रौद्योगिकी संस्थान जम्मू
INDIAN INSTITUTE OF TECHNOLOGY JAMMU
विद्याधनं सर्वधन प्रधानम्

Indian Institute of Technology Jammu
Department of Electrical Engineering
Jagti, NH-44, PO Nagrota, Jammu, J&K 181221

Advt. No.: IITJMU/R&C/RP00177/A-18 **Dated: 23-Feb-2024**

Advertisement for the Research Project Staff in VLSI Design

Applications are invited from highly motivated candidates for the position of Junior Research Fellow to work on the sponsored research project of **Ministry of Electronics & Information Technology (MeitY)** under **Chip to Startup (C2S)** initiative for the project entitled **"Implantable Pacemaker Chip (iPACE-CHIP)"** at Department of Electrical Engineering, Indian Institute of Technology Jammu.

Aim of Project: The aim of the project is to design and fabricate the next generation chip (iPACE-CHIP) for implantable pacemaker to be used in the commercial product of Shree Pacetronix Ltd. with enhanced features.

Nature of job: Applicant should be capable of handling a project and carryout the research work in the area of Analog and Digital IC Design using industry standard integrated circuit technology including SCL180nm.

S. No.	Position	No. of Posts	Minimum Qualification	Salary per Month
1	Junior Research Fellow (JRF)	01 (One)	Refer essential qualification and criteria	Rs. 37,000/- + HRA as applicable

Essential Qualification and Criteria

1. Junior Research Fellow (JRF) position:

A. M.E./M.Tech./MS(R) or equivalent degree in ECE/EE/Microelectronics/VLSI Design/ Embedded Systems and allied subjects with 65% marks. 5% marks relaxation for ST/SC/PH candidates. Students awaiting results may also apply.

OR

Candidates with B.E. /B.Tech/M.Sc. in ECE/EE/Electronics/Microelectronics/VLSI Design/Embedded Systems and allied subjects with 65% marks.

B. Qualified in any of the following National eligibility test/exams:

i. GATE
ii. CSIR-UGC NET including lectureship (Assistant Professorship)
iii. National-level examination conducted by Central Govt. Departments and their agencies and Institutions such as DST, DBT, DAE, DOS, DRDO, MHRD, ICAR, ICMR, IIT, IISc, IISER, etc.

C. Upper age limit: 30 years for JRF. Age relaxation is applicable for SC/ST/OBC/PH/women candidates as per the norms.

D. Candidates having experience on Verilog/VHDL and EDA tools (Cadence, Synopsys, etc) will be given preference.

Application Process:

Duly filled application form along with the requested details, scanned copies of certificates, other supporting documents, should be uploaded through the online portal (https://apply.iitjammu.ac.in/#/home) and should email to **ambika.shah@iitjammu.ac.in** with the subject line **"Application for JRF in VLSI Design"** latest by **March 02, 2024**. Please apply through the [contract/project staff/JRF/SRF] tab on the referred application portal.

Important Points:

1. Post is initially for one year, which may be extended upto the duration of the project based on the satisfactory performance.
2. The applicant will be responsible for the authenticity of the information, other documents, and photographs submitted.
3. Merely possessing the prescribed qualification does not ensure that the candidate would be called for an Interview. The candidates may be shortlisted based on merit and need for the project.
4. Only shortlisted candidates will be called for the interview. The time and date of the interview will be informed to the shortlisted candidates by e-mail.
5. The interview will be conducted in online mode.
6. Candidates who are already employed should produce a relieving certificate from their employers if selected.
7. The selected candidate will be encouraged to apply for the PhD program if he/she satisfies all the criteria for PhD admission. However, the candidate can only be selected through the regular admission process for the PhD program at IIT Jammu.
8. Candidate must upload all the documents with respect to educational qualification, Experience etc.

Principal Investigator:
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